This listing of the claims replaces all prior versions, and listings of claims in the application:

LISTING OF THE CLAIMS

1. (Currently amended) A reusable software block stored in a computer-readable memory, the reusable software block comprising:

a device hardware abstraction software layer adapted to configure multiple instantiations of a peripheral device within an integrated circuit, the hardware abstraction software layer defining, relative to a variable base address received as a parameter passed to the device hardware abstraction software layer, offset values for registers of the peripheral device and defining a data structure for the peripheral device that accesses the registers of the peripheral device relative to the variable base address; and;

a platform hardware abstraction software layer defining an address map of the integrated circuit ~~system~~ comprised of a plurality of base addresses, the platform hardware abstraction software layer adapted to configure each instantiation of the peripheral device via calls to the device hardware abstraction software layer, the calls to the device hardware abstraction software layer each passing a one of the plurality of base addresses that correspond to an instantiation of the peripheral device to the device hardware abstraction software layer.

2. (Previously presented) The reusable software block of claim 1 wherein the device hardware abstraction software layer comprises:

memory register locations adapted to be configurable during initialization of the system; and

an interrupt configuration, which is configured for the peripheral device during initialization of the system.

3. (Previously presented) The reusable software block of claim 2 wherein the memory register locations and the interrupt configuration define the data structure of the peripheral device using variables.

4. (Previously presented) The reusable software block of claim 1 wherein the data structure of the peripheral device is defined in the device hardware abstraction software layer using variables, the address map comprising:

memory locations associated with each instantiation of the peripheral device.

5. (Previously presented) The reusable software block of claim 4 wherein the platform hardware abstraction software layer initializes each memory location according to the memory map.

6. (Previously presented) The reusable software block of claim 1 wherein the data structure of the peripheral device is defined in the device hardware abstraction software layer using variables, the platform hardware abstraction software layer comprising:

an interrupt configuration corresponding to interrupt connections for a particular implementation of the peripheral device.

7. (Previously presented) The reusable software block of claim 6 wherein the interrupt configuration initializes each interrupt connection of the particular implementation of the peripheral device according to the interrupt configuration.

8-15 (Canceled)

16. (Currently amended) A system for instantiating multiple instantiations of a peripheral device within an integrated circuit, the system comprising a single configurable code block, which is stored in a computer-readable memory and comprises:

a device hardware abstraction software layer defining a configurable data structure for the peripheral device relative to a variable base address received as a parameter passed to the device hardware abstraction software layer, the configurable data structure accessing the registers of the peripheral device relative to the variable base address; and

a platform hardware abstraction software layer adapted to define a base address ~~configure the structure~~ of each particular instantiation of the peripheral device and configure each particular instantiation of the peripheral device via calls to the device hardware abstraction software layer, the calls to the device hardware abstraction software layer each passing a defined one of a plurality of base addresses that correspond to each particular instantiation of the peripheral device.

17. (Previously presented) The system of claim 16 wherein the device hardware abstraction software layer comprises:

memory register locations adapted to be configurable during initialization; and

an interrupt configuration, which configures at least one interrupt connection for the peripheral device during initialization of the system.

18. (Previously presented) The system of claim 17 wherein the memory register locations and the interrupt configuration define the structure of the peripheral device using variables.

19. (Previously presented) The system of claim 16 wherein the configurable structure of the peripheral device is defined in the device hardware abstraction software layer using variables, the platform hardware abstraction software layer comprising:

a memory map of memory locations of the peripheral device corresponding to a particular implementation of the peripheral device, the memory map adapted to replace the variables with unique memory locations for each instantiation.

20. (Previously presented) The system of claim 16 wherein the configurable structure of the peripheral device is defined in the device hardware abstraction software layer using variables, the platform hardware abstraction software layer comprising:

an interrupt configuration corresponding to interrupt connections for a particular implementation of the peripheral device, the interrupt configuration adapted to replace the variables with values that define unique interrupt connections for each instantiation.